Current Conduction and Dielectric Behavior of High k-Y_2O_3 Films Integrated with Si Using Chemical Vapor Deposition as a Gate Dielectric for Metal-Oxide-Semiconductor Devices

A.C. RASTOGI & S.B. DESU

Department of Electrical & Computer Engineering, 201 Marcus Hall, University of Massachusetts, Amherst, MA 01003, USA

Abstract. Integration of Y_2O_3 high-k thin film over Si as gate dielectric in high performance CMOS and high-density MOS memory storage capacitor devices is described. Y_2O_3 film growth by low-pressure chemical vapor deposition induces interfacial reactions and complex SiO_{2-x} layer growth. It has a graded structure, in crystalline-SiO_2 form at Y_2O_3 side and amorphous SiO_{2-x} form at Si side. MIS devices based on Y_2O_3/SiO_2-SiO_{2-x} composite dielectric integrated with Si show high frequency C-V behavior indicative of inversion to accumulation changes in capacitance. Observed bi-directional hysterisis in C-V is detrimental to the functioning of storage capacitor in memory function. Detailed investigation of this effect led to understanding of gate bias controlled emission of carriers as responsible mechanism. Observed anomalous increase in inversion capacitance at low frequency is attributed to additional charges transferred from SiO_{2-x}/Si interface states. Leakage current and injected charge carrier transport across bilayer interface is dominated by Poole-Frankel (PF) process at low fields and by Fowler-Nordhiem (FN) at high fields. This investigation provides a greater understanding of the complex nature of integration of Y_2O_3 films.

Keywords: Y_2O_3 films, high k oxides, LPCVD, MOS storage capacitor

1. Inroduction

Scaling down of feature size of the metal-oxide-semiconductor (MOS) devices requires a concomitant reduction in equivalent SiO_2-dielectric thickness to realize desired capacitance density. For 0.13 and 0.07 micron technologies, respective equivalent oxide thickness of 2–3 nm and <1.5 nm are required [1]. Thinner SiO_2 gate dielectric poses complex integration issues related to the penetration of impurities such as boron through thin gate [2], nonuniform oxide growth and reliability. Further, the leakage current increases exponentially from 1×10^{12} A/cm^2 at ~ 3.5 nm to 1×10^0 A/cm^2 at ~ 1.5 nm [3, 4]. Exceptionally high leakage currents in CMOS and memory storage capacitor devices with ultra thin gate dielectric contribute to high power dissipation, loss of device lifetime and unreliable performance [5]. Since CMOS and storage capacitor devices are designed with specific gate capacitance, a higher gate capacitance is possible with thicker gate dielectric using a higher dielectric constant (high-k) gate material. Thicker dielectric layer prevents gate leakage current arising from direct quantum mechanical tunneling provided high-k material has large band gap that yields high barrier height. Several high-k gate oxides Ta_2O_5 [6], CeO_2 [7], ZrO_2 [8], HfO_2 [9], $BaSrTiO_3$ [10] and Y_2O_3 [11, 12] have been widely studied. Conceptually, high-k materials are attractive and physics of CMOS device operation with high-k gate is simple, but technologically, its integration with Si has several problems. High temperature processing of oxide gates induces unwanted reactions leading to interfacial SiO_2 or silicide formation. Both contribute to reduction in dielectric constant and hence to ineffectiveness of high-k gate. As extrinsic gate oxides are polycrystalline, localized asperities and narrow grain boundaries are high field sites that result in excessive leakage currents [13, 14]. A way around is to use a interfacial SiO_2

buffer layer which reduces leakage current [13–16] but a reduced effective dielectric constant of composite gate requires management of relative high-k-SiO$_2$ thickness for application as gate dielectric in CMOS devices.

A relatively unexplored aspect of high-k-SiO$_2$ interface is interface defect states, charge trapping and C-V hysteresis due to structural discontinuities between two layers of differing electronic properties. Further, in integration of high-k gate oxide processing, interfacial SiO$_2$ growth is structurally different from thermally oxidized bare Si wafers [11, 12]. This paper presents a study of Y$_2$O$_3$/SiO$_{2-x}$ bilayer gate dielectric integrated over p-Si wafers using low-pressure chemical vapor deposition (LPCVD) technique and a detailed discussion of the results of dielectric properties and leakage current conduction in metal-insulator-semiconductor (MIS) devices structures.

2. Experimental

Y$_2$O$_3$ dielectric thin films were deposited on p-Si (100) wafers by LPCVD process in a horizontal hot wall reactor. Yttrium di-pivalyol methanate (YDPM) metallo-oraganic complex was used as precursor. YDPM vapor formed by heating solid source at 160°C were transported to the reaction zone by an oxygen flow at 10 sccm. Precursor vapors decompose to form Y$_2$O$_3$ film over Si substrate held at 580°C and ~1 Torr pressure. YDPM flux and deposition time determines Y$_2$O$_3$ film thickness. Post growth insitu annealing of Y$_2$O$_3$ film/Si structure thus grown was carried out at 600°C for ~45 min within reactor to improve the stochiometry Y$_2$O$_3$ film and to minimize defects due to oxygen vacancy. Details of the LPCVD process are described elsewhere [11]. Y$_2$O$_3$ film thickness determined by ellipsometry was 52 nm. Composition of Y$_2$O$_3$ film and of SiO$_{2-x}$ at interface was analyzed by Auger electron spectroscopy. Dielectric and electrical properties of Y$_2$O$_3$ gate dielectric were studied in a MIS structure. Charge trapping at interface was studied in electron injection mode by selectively applying negative bias at gate electrode. Electrical properties were measured by capacitance-voltage (C-V) measurements at various frequencies under varying DC gate bias. For leakage-current measurements, a slow varying voltage ramp is impressed at top Al electrode of appropriate polarity for accumulation and inversion modes.
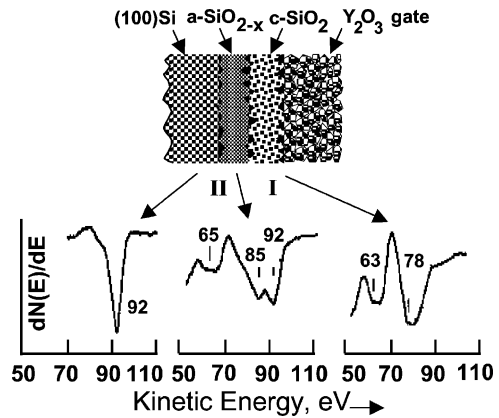

Fig. 1. Auger electron spectra and schematic cross-section of compositionally graded silicon oxide interface layer emerging from integration Y$_2$O$_3$ gate dielectric over Si.

3. Results and Discussion

3.1. Interface Structure

In situ annealing at 600°C during integration of 52 nm Y$_2$O$_3$ film over Si results in the growth of an interfacial silicon oxide layer. Auger studies presented in Fig. 1 show that silicon oxide buffer layer has a graded structure differing in composition at interface-I towards Y$_2$O$_3$ side and interface-II towards Si wafer side. This is inferred from characteristic features of Si—O bonding as revealed by Si(L$_{23}$VV) transitions at various depths beneath Y$_2$O$_3$ film on exposure by chemical etching of Y$_2$O$_3$ film and towards the Si side by depth profiling using ion beam etching. AES spectra at interface-I between Y$_2$O$_3$ and silicon oxide has two principal peaks at 78 and 63 eV and none at 92 eV due to free Si. Thus, Si is in the bonded state and Si (L$_{23}$VV) transitions are interpreted as due to O$_{2p}$-Si$_{3s/3p}$ and O$_{2s}$-Si$_{3s/3p}$ Auger transitions [17]. Further O(K$_1$L$_1$L$_1$) transitions seen at 503 and 483 eV confirm bonded oxygen presence. A strong Auger line at 78 eV suggests SiO$_4$ tetrahedra are arranged in a compact ring like structure of SiO$_4$ bonds forming a 3-D network [18]. This is associated with a more ordered SiO$_2$ phase. The ordered ring structure in such crystalline SiO$_2$ may typically extent to ~10 SiO$_2$ structural units such as in a coesite SiO$_2$ phase [19]. Si Auger line features continually change as probed in deeper layers of interface. At a certain depth towards Si surface side, the 63 eV peaks broadens and moves to 65 eV but 78 eV line disappears. Additional line features that

emerge at 85 and 92 eV suggest a lower degree of SiO_4 coordination. The 85 eV Auger line is associated with defects and disorder in SiO_2 [20] possibly from broken Si—O bonds at localized regions of $Si-SiO_4$ linkages forming a network of small size $Si-O_3-O$ tetrahedra [21]. Further, broad features extending from 65 to 71 eV show a mixture of different oxidation states of silicon conforming to a disordered SiO_{2-x} phase. Profiling the AES spectra further towards the Si substrate, the 85 eV transition line gradually diminishes and disappears entirely at Si surface. A stronger 92 eV transition arises at this stage from the $Si-Si_4$ coordination due to single crystal Si substrate. In summary, the AES observations support that silicon oxide layer formed at interface has a graded composition. A more ordered coesite like crystalline $c-SiO_2$ forms underneath Y_2O_3 and an amorphous $a-SiO_{2-x}$ growth consisting of high percentage of unlinked $Si-O_4$ tetrahedra towards Si surface. Using calibration standard for ion beam etching it was established that silicon oxide thickness is $\sim$8 nm and both structural forms are of comparable thickness.

3.2. Frequency Dependent C-V Characteristics

Figure 2(a) shows typical C-V characteristics of MIS device with bilayer Y_2O_3-SiO_{2-x} gate dielectric. High, 1 MHz frequency curve shows flat band voltage V_{FB} of −4.8 V which predicts effective positive charges $\sim$4.5 × 10^{12} cm^{-2}. This charge, due to oxygen vacancy defects in Y_2O_3 films is about 4 times larger than Y_2O_3 films formed by electron beam method with-

out the interfacial SiO_2 layer. Additional charge density in CVD formed Y_2O_3 films are due to the bilayer $c-SiO_2/a-SiO_{2-x}$ character of interfacial silicon oxide layer. Initial C-V curve is obtained by driving the MIS structure into accumulation from the strong inversion direction. Hysteresis is seen as reversing the dc bias direction shifts C-V curve towards positive bias. This indicates a change in the effective charge density by inclusion of additional negative charges. Enhanced hysteresis is caused by electron injection into Y_2O_3 at negative bias during +5 to −10 V sweep and capture by defect states, which results in negative charge generation in the Y_2O_3 dielectric film. Since the extent of hysteresis effect is not exacerbated when strong negative voltage bias is applied, it appears that trapping states are not related to generation of defects in Y_2O_3 through voltage stress. Density of bulk traps in Y_2O_3 is less likely to change with film thickness, increased hysteresis is reflective of initial formation of additional trapping states at Y_2O_3/SiO_2 and/or SiO_2/SiO_{2-x} interfaces. Nature and existence of interface charge states, generation, recombination traps in the depletion region as well as response of bulk defect related trap states are elucidated by C-V measurements in the intermediate (0.5–0.05 MHz) and low (10–0.1 KHz) frequency domains. Bilayer Y_2O_3/SiO_{2-x} gate dielectric has two interfaces, one between two dissimilar Y_2O_3/SiO_2 layers and one of graded composition SiO_{2-x} with Si. Defect related trap states in the bulk of composite dielectric are characteristically different from the properties of individual layers. Hysteresis effect manifests due to capture-emission of injected minority carriers by fast traps at Y_2O_3/SiO_{2-x} interface. Minority carrier electrons emitted by traps in the reverse bias sweep introduce excess negative charges, shifting C-V curve towards positive voltage direction. Asymmetric nature of hysteresis is due to exchange of charges between interface traps or Si surface due to graded structure of interfacial SiO_{2-x}. Accumulation capacitance rises initially, followed by a decrease as increasing gate bias exceeds depletion threshold. With voltage sweep, as quasi Fermi level lowers through Si band gap, a rapid discharge of minority carriers from traps is responsible for increased capacitance. Usually, a peak in accumulation capacitance is not seen in single phased thermally grown $a-SiO_2$ gate. A reduction in hysteresis, inferred from reduced lateral shift in flat band voltage, seen as measurement frequency is lowered indicates higher percentage of density of trap states have a smaller time constant. Further, interface trap states are
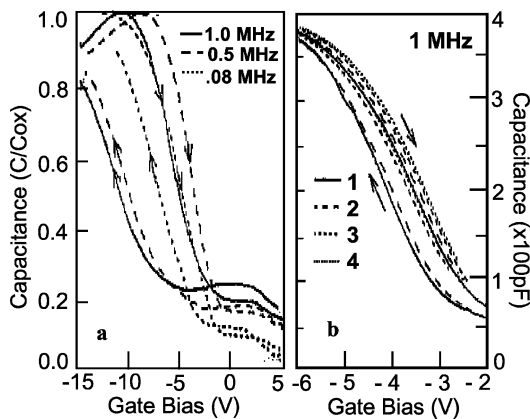

Fig. 2. (a) Frequency dependent C-V curves and hysteresis in MIS device with c-Y_2O_3/c-(SiO_2-a-SiO_{2-x}) gate dielectric. (b) hysteresis shifts in repetitive high frequency (1 MHz) C-V curves.

shallow in energy as captured minority electrons are emitted without a residual charge. Therefore, initial C-V and hysteresis curves repeat itself. To confirm this, in a separate experiment, charges are partially emitted from traps by applying smaller positive dc bias during reverse (depletion direction) gate bias scan. When forward (accumulation direction) C-V curve is retraced, it shifts towards positive direction from the initial curve, which implies inclusion of additional negative charge which had remained un-emitted from the traps due to insufficient bias. Reverse traced hysteresis curve is also shifted positively for the same reason. As seen from Fig. 2(b) curves 1–4, under repeated voltage cycling each time curves shift positively until an equilibrium state is observed. At this stage, electron capture and emission in the two gate bias directions are parallel and voltage shifts are no longer possible as all available traps are saturated. It shows that interface traps are shallow and distributed in energy across Si band gap.

Low (≤ 10 KHz) frequency C-V curves are shown in Fig. 3. As measurement frequency gradually lowers, inversion state forms at lower bias and inversion capacitance increases. In intermediate frequency (0.5–0.05 MHz) C-V, inversion layer forms at positive gate bias and minority carriers restrict further increase in the electric field in the depletion region causing depletion capacitance to remain constant. At lower (10–0.1 KHz) frequencies, minority carriers (electrons) as
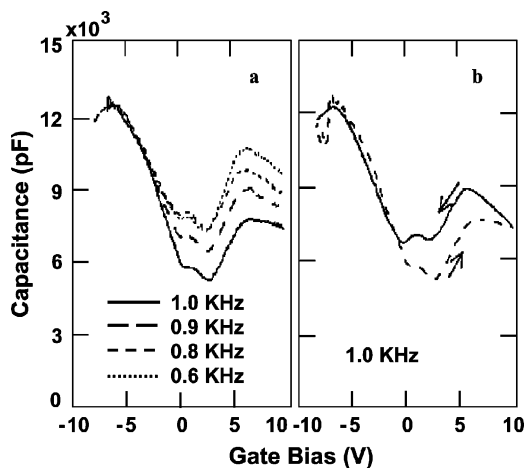
well as interface traps show capacitive response and inversion capacitance rises. Minority carriers in inversion layer and interface traps begin to respond to a slowly changing ac signal but are unable to follow any high frequency signal [22]. Dispersion in inversion region capacitance is therefore due to large response time of minority carriers. Low frequency C-V curves in Fig. 3(a) are similar to standard metal-oxide-semiconductor (MOS) quasistatic C-V curves except that in bilayer Y_2O_3/SiO_{2-x} gate dielectric this occurs at high, 0.8–0.3 KHz as compared to much lower 0.01–0.005 KHz frequencies for standard MOS. This is explained by a mechanism, which involves additional charge flow into inversion layer. Y_2O_3/SiO_{2-x} bilayer gate dielectric has fast interface trap states having effective negative charge centers. Inversion layer essentially forms inside Si beyond the gate region. Charged trap states in bilayer dielectric adjacent to SiO_{2-x}/Si interface can transfer charge to inversion layer. Inversion layer in p-Si MIS device consists of minority carrier electrons, whose response to applied ac signal largely determines the steady state C-V behavior. Frequency dependence of inversion capacitance thus depends on the manner by which minority carriers are injected and are driven out of the inversion layer. A possible mechanism is generation recombination process in the depletion layer via interface states located at Y_2O_3/SiO_{2-x} -Si. Thus, frequency dependence arises from energy loss due to change in the occupancy of inversion layer by ac signal. During positive voltage cycle, electrons are drawn to inversion layer that come by generation at interface traps with holes thermalized into Si bulk. In case of Y_2O_3/SiO_{2-x} gate dielectric, electrons demanded by inversion layer are supplied by generation without loss at a faster rate; typically at $\sim$0.8–0.6 KHz compared to much slower rate < 0.02 KHz in standard MOS. As frequency increases, generation rate from interface traps is unable to keep pace with the ac signal. Similarly, at the negative voltage cycle, electrons are driven out of the inversion layer, which then recombine through traps. At > 0.8 KHz, recombination rate is unable to match electron ejection from inversion layer. As a result, change in the occupancy of minority carrier electrons in inversion layers, its charge and hence capacitance changes. These changes in the interface traps occupancy by dc gate bias are reflected in C-V curves.

Origin of density of interface trap states of varying time constants in LPCVD formed Y_2O_3/SiO_{2-x} gate dielectric is not clear. These states appear related to

Fig. 3. (a) Frequency dependence of C-V curves for MIS device at 1.0, 0.9, 0.8 and 0.6 KHz under bias scanned from accumulation to inversion state, (b) hysteresis in C-V curves for MIS device at 1.0 KHz.

interface defects due to broken bonds, local distortion in bond angles and lengths at Y$_2$O$_3$/SiO$_{2-x}$ interface. A non-ideal interface between crystalline Y$_2$O$_3$ and c-SiO$_2$ or graded c-SiO$_2$-a-SiO$_{2-x}$ is riddled with macroscopic defects, composition gradient and stresses arising from bonding mismatch. These contribute to inclusion of fast states having different time constants. These states would also manifest at the interface as randomly distributed localized charged interface traps. Negative charge in the bilayer gate dielectric increases as these traps are activated when frequency is changed. It seems that these traps are negatively charged just as acceptor states are when filled.

3.3. Hysteresis in Low Frequency C-V Curves

Figure 3(b) shows hysteresis effect in low frequency C-V curves. Inversion capacitance is always higher when C-V curve is traced from inversion towards accumulation region. Further, C-V curves show peaks at the edge of weak inversion and in the inversion region. These observations are ascribed to two facts, (1) interface state show a non-equilibrium behavior and (2) trap states are not localized only at the interface but could also spatially distributed in the dielectric closer to the interface. When voltages scan direction is from accumulation to inversion, inversion layer has to form beyond the bias level for depletion state. Inversion layer forms due to minority carriers (electrons) and is therefore affected by minority carrier generation through interface traps. For equilibrium, formation of inversion layer, magnitude of displacement current during gate bias sweep from negative to positive direction should be relatively much smaller than the generation rate. When this condition is violated, process of formation of inversion layer is impeded and deviates from equilibrium state. Consequently, capacitance in the inversion region lowers as in indeed seen in Fig. 3(b). On the other hand, gate bias sweep from strong inversion direction starts from a well-formed inversion layer. Bias scans in this direction results in a small forward bias across MIS device causing a forward current higher than the displacement current in the reverse direction. This forward current shifts C-V curves towards the scan direction-giving rise to hysteresis. As gate bias reduces, electrons in the inversion layer begin to recombine with holes in Si and capacitance reduces. Under non-equilibrium conditions, excess charge in the inversion layer due to interface traps discharges rapidly into Si. This causes

formation of peak in measured C-V curves in the depletion and weak inversion regions. Its magnitude and position at gate bias depends on interface trap density and excess minority carrier charge induced by these into inversion layer.

3.4. Leakage Current Conduction and Mechanisms

Observed leakage current density $\sim 1 \times 10^{-6}$ A/cm^2 at 200 KV/cm is rather high for device operation. Understanding of the complex conduction mechanism in bilayer gate dielectric of different energy gaps and dielectric constants is important to alleviate the problem in MIS devices. I-V data were analyzed by considering separate field distribution across Y$_2$O$_3$ and SiO$_2$. Plotting I-V data according to Poole-Frankel (P-F) and Fowler-Nordhiem (F-N) tunneling processes identified dominating current conduction mechanism. Accumulation and inversion mode current conduction follows P-F mechanism as shown in Fig. 4(a). It may be recalled that gate dielectric has a bilayer 52 nm Y$_2$O$_3$ and 8 nm c-SiO$_2$-a-SiO$_{2-x}$ graded composition. Inferred high effective $k \sim 32\varepsilon_0$ is therefore due to non-uniformities in Y$_2$O$_3$ bulk and at interface. Conduction process at c-SiO$_2$-a-SiO$_{2-x}$ interface is evaluated when Y$_2$O$_3$ film was selectively etched and contacts were made directly to silicon oxide. As shown in Fig. 4(b), current conduction through interfacial silicon oxide layer follows F-N
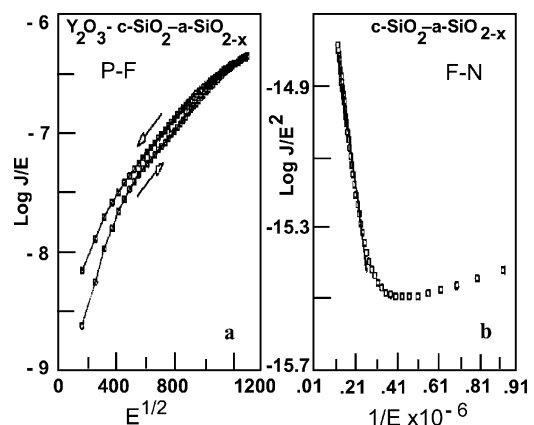

Fig. 4. (a) Leakage current behavior of MIS device with c-Y$_2$O$_3$/(c-SiO$_2$-a-SiO$_{2-x}$) through interfacial silicon oxide layer gate dielectric plotted for P-F conduction mechanism. (b) Leakage current behavior of MIS device with c-SiO$_2$-a-SiO$_{2-x}$ gate dielectric plotted for F-N conduction mechanism.
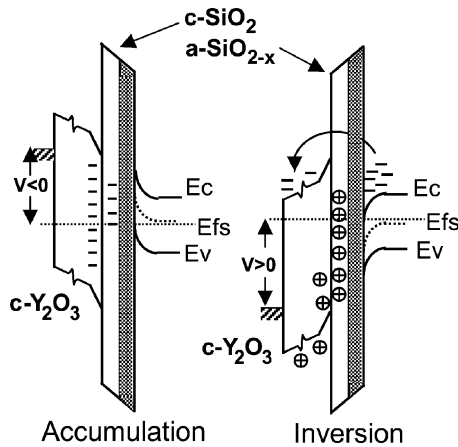
Fig. 5. Energy band diagram of MIS device based on bilayer c-Y$_2$O$_3$/(c-SiO$_2$-a-SiO$_{2-x}$) gate dielectric showing carrier transport in the accumulation and inversion bias states.

process in the inversion mode at high fields. Barrier height calculated from straight line fit of high electric field data in Fig. 4(b) is 0.48 eV. Low value is due to defect states as electron tunneling is mediated through these states.

Further understanding of the current conduction process is realized from energy band diagram in Fig. 5. In accumulation, electrons inject into Y$_2$O$_3$ dielectric from top Al electrode and conduct according to P-F mechanism. At Y$_2$O$_3$/SiO$_2$ interface, electrons face a higher barrier and at high field are transported across SiO$_{2-x}$ into conduction band of Si by F-N mechanism. With non-stoichiometric SiO$_{2-x}$, electrons conduct through interface states due to defects and emit into Si conduction band to flow across to the other electrode. In inversion mode conduction, electrons are injected at Si substrate and conduct through SiO$_{2-x}$ layer and then into Y$_2$O$_3$ layer for collection at top Al electrode as shown by band alignment in Fig. 5. Due to interfacial defects, in conjunction with Y$_2$O$_3$ layer, electrons get emitted via defect states directly into the conduction band of Y$_2$O$_3$ and swept by bias field. Conduction process is therefore dominated neither by P-F emission in Y$_2$O$_3$ nor by F-N in SiO$_{2-x}$. In case of thin SiO$_{2-x}$ electrons are emitted into mid gap of Y$_2$O$_3$ by tunneling and are transported across the Y$_2$O$_3$ by P-F conduction. In this case therefore both inversion and Y$_2$O$_3$ layer dominates accumulation mode conduction. To reduce leakage current, minimization of defects due to graded SiO$_{2-x}$ structure is important.

4. Conclusions

Interfacial growth of SiO$_{2-x}$ film is an inevitable consequence of integration of extrinsic high-k Y$_2$O$_3$ film over Si as a gate dielectric for fabrication high performance CMOS or memory capacitor devices. SiO$_{2-x}$ layer has two interfaces differing in structure and composition at Y$_2$O$_3$ and Si sides, which depends critically on processing temperature and the thickness of Y$_2$O$_3$ film. Oxide charge density, interface trap states, bidirectional hysteresis and electron trapping observed in MIS devices based on extrinsic Y$_2$O$_3$ high-k dielectric are affected by composition of interfacial SiO$_{2-x}$. Frequency dispersion and hysteresis effects in C-V curves indicate trapping states of varying time constant distributed across Si band gap due to SiO$_{2-x}$ composition gradation that could be detrimental for device use as bilayer gate dielectric. Leakage current behavior is also affected by structure and composition of SiO$_{2-x}$ at interface. Current transport in accumulation mode is dominated by P-F process across Y$_2$O$_3$ layer at low fields and by F-N at high fields. Low F-N barrier heights are encountered due to defects in the SiO$_{2-x}$ layer in the SiO$_{2-x}$/Si structure.

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